PENDING CLAIMS:

1. An integrated circuit structure fabrication method, comprising:

forming n-type and p-type regions within a substrate;

forming an oxidation barrier on a surface of the substrate over the n-type and p-type regions;

forming a first patterned layer which exposes first isolation areas in the n-type region and which covers substantially all of the p-type region and active device areas in the n-type region;

removing portions of the oxidation barrier layer exposed by the first patterned layer to expose the first isolation areas;

implanting a first channel-stop dopant into the first isolation areas exposed by the first patterned layer and the oxidation barrier layer;

removing the first patterned layer;

forming a second patterned layer which exposes second isolation areas in the p-type region and which covers substantially all of the n-type region and active device areas in the p-type region;

removing portions of the oxidation barrier layer exposed by the second patterned layer to expose the second isolation areas;

implanting a second channel-stop dopant into the second isolation areas exposed by the second patterned layer and the oxidation barrier layer;

removing the second patterned layer; and

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growing a field oxide on the first and second isolation areas where exposed by the oxidation barrier layer in a single oxidation step.

32. The method of claim 1, wherein the first isolation areas are protected by only the second patterned layer during implantation of the second channel-stop dopant into the second isolation areas.

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33. The method of claim 1, wherein the oxidation barrier overlies an oxide layer which is patterned together with the oxidation barrier using the first and second patterned layers to expose the first and second isolation areas.

34. The method of claim 33, wherein the oxidation barrier overlies a polysilicon layer on the oxide layer which is patterned together with the oxidation barrier and the oxide layer using the first and second patterned layers to expose the first and second isolation areas.

35. The method of claim 1, wherein critical dimensions for the active device areas in the p-type region are selected independently from critical dimensions selected for the active device areas in the p-type region.

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36. The method of claim 1, further comprising:

prior to removing the first patterned layer, etching the substrate through the first patterned layer to form recesses in the first isolation areas in the n-type region.

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37. The method of claim 1, further comprising:

prior to removing the second patterned layer, etching the substrate through the second patterned layer to form recesses in the second isolation areas in the p-type region.

60 38. A method of forming an integrated circuit structure, comprising:

forming an active stack over two adjacent wells having opposite conductivity types within a substrate;

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patterning the active stack using a first patterned layer to expose isolation regions within a first well having a first conductivity type;

implanting a channel-stop into the exposed isolation regions within the first well masked by the first patterned layer, wherein the first patterned layer protects active device areas in the first well and substantially all of the second well during the implant of the channel-stop in the exposed isolation regions within the first well;

removing the first patterned layer;

patterning the active stack using a second patterned layer to expose isolation regions within the second well having a second conductivity type;

implanting a channel-stop into the exposed isolation regions within the second well masked by the second patterned layer, wherein the second patterned layer protects active device areas in the second well and substantially all of the first well during the implant of the channel-stop in the exposed isolation regions within the second well;

removing the second patterned layer; and

growing a field oxide on the isolation regions within both the first and second wells with a single oxidation step.

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39. The method of claim 38, wherein the isolation regions within the first well are protected by only the second patterned layer during implantation of the channel-stop into the isolation regions within the second well.

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40. The method of claim 38, wherein the active stack further comprises:

a nitride layer overlying an oxide layer, wherein the nitride and oxide layers are patterned together using the first and second patterned layers to expose the first and second isolation areas.

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41. The method of claim 40, wherein the active stack further comprises:

a polysilicon layer between the nitride and oxide layers, wherein the polysilicon layer is patterned together with the nitride and oxide layers using the first and second patterned layers to expose the first and second isolation areas.

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42. The method of claim 38, wherein critical dimensions for the active device areas in the first well are selected independently from critical dimensions selected for the active device areas in the second well.

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43. The method of claim 38, further comprising:

prior to removing the first patterned layer, etching the substrate through the first patterned layer to form recesses in the exposed isolation regions within the first well.

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44. The method of claim 38, further comprising:

prior to removing the second patterned layer, etching the substrate through the second patterned layer to form recesses in the exposed isolation regions within the second well.

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45. The method of claim 38, wherein the first well is an n-well and the second well is a p-well.

46. An integrated circuit structure, comprising:

an active stack over two adjacent wells having opposite conductivity types within a substrate, wherein the active stack has openings therethrough over isolation regions within a first well having a first conductivity type and over isolation regions within the second well having a second conductivity type;

C2 a channel-stop within the substrate beneath the isolation regions within the first well; and

a patterned masking layer on the active stack and on the substrate within the isolation regions within the first well, wherein the patterned masking layer has openings therethrough over the isolation regions within the second well.

47. The integrated circuit structure of claim 45, further comprising:

a channel-stop within the substrate beneath the isolation regions within the second well.